**Mission Requirements Document (MRD)**

**EXAMPLE-SAT1**

**On Board Computer (OBC)**

**Document Control**

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**Revision History**

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# Introduction

This document outlines the objectives, scope, and requirements for the EXAMPLE-SAT1, a BIRDS-based 1U CubeSat project. The MRD serves as the foundation for the design, development, testing, and validation of the spacecraft’s On-Board Computer (OBC) and associated subsystems.

# Mission Overview

## Mission Statement & Objectives

The mission aims to replicate the BIRDS3 OBC module with local materials to demonstrate that the BIRDS On-Board Computer (OBC) module is reliable, cost-effective, and can be redesigned, built, and tested in this example country. This OBC will manage satellite operations, data handling, and payload support, ensuring the mission’s overall success while providing a hands-on learning experience for students and supporting the global CubeSat community.

Objectives:

* Demonstrate technology transfer readiness for 1U cubesat missions using the BIRDS platform.
* Collect telemetry and health data to validate system performance.
* Engage students in hands-on satellite development and operations.

## Mission Profile

|  |  |  |
| --- | --- | --- |
| Parameter | Value | Rationale |
| Orbit Type | LEO (400 km, 51.6°) | Matches ISS deploy altitude for Birds program |
| Mission Duration | 2 years / design to operation | Optimum student cycle |
| Ground Stations | 1 static, 1 mobile | Least cost |

# System Specifications

## Functional Requirements

1. OBC shall provide command & data handling for payload, EPS, COM, ADCS.
2. OBC shall interface via SPI, UART.
3. OBC shall support at least **100 kB** telemetry buffer.

## Performance Requirements

|  |  |  |
| --- | --- | --- |
| Item | Requirement | Verification Method |
| CPU Throughput | ≥ TBD MIPS | Analysis / Test |
| RAM | ≥ 500 kB | Inspection |
| Mass | ≤ 0.90 g | Weighing |
| Power (average) | ≤ 12 mW | Test |

## Environment & Reliability

* Radiation tolerance: **≥ 10 krad (TID)**; latchup immune to 60 MeV cm²/mg.
* Operating temperature: 20 °C to +60 °C.
* Vibration: per NASAGEVS launch load envelope.

# Product Breakdown Structure (PBS)

Level 0: EXAMPLE-SAT1

  └── Level 1: OBC Subsystem

        ├── CPU Module

        ├── Power Regulation & Reset Circuitry

        ├── Data Storage (NAND Flash / FRAM)

        ├── I/O Interface Board

        └── Flight Software (FSW)

# Block Diagram

**Placeholder:** High level functional block diagram TBD

# Backplane Pin Allocations

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Connector | Pin No. | Signal Name | I/O | Description | Subsystem |
| J1 (OBCEPS) | 1 | +5 V | Pwr Out | Regulated power to EPS | EPS |
|  | 2 | I²CSCL | I/O | I²C clock | ADCS |
| ... | 3 | ... | ... | ... | ... |
|  |  |  |  |  |  |

# Data Budget

## Data Source

|  |  |  |  |
| --- | --- | --- | --- |
| Source | Description | Data Rate (kbps) | Estimated Daily Data (MB) |
| Payload Camera | Earth observation images | 54600 | 2 |
| Housekeeping Telemetry | Satellite health and status | 4300 | 0.4 |
| ADCS Sensor Logs | Attitude control sensor data | 25400 | 1.3 |
| Debug/Logs | Event and error logging | 4300 | 0.2 |

## Data Storage Allocation

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| TM ID | Parameter | Units | Update Rate | Source |
| 0x01 | OBC Board Temp | °C | 10 s | ADC Ch 3 |
| 0x02 | 5 V Bus Voltage | V | 1 s | ADC Ch 1 |
| ... | ... | ... | ... | ... |

# Operation Scenarios

1. **Launch & Early Orbit Phase:** OBC powers on in safe mode; beacons housekeeping; awaits ground commands.
2. **Nominal Mission Mode:** OBC schedules payload operations; manages data storage; downlinks data via COM.
3. **Safe Mode:** Trigger on anomaly; disables payload; minimizes power; transmits safety beacons.
4. **Deorbit Phase:** Execute end-of-life procedures, clear memory, transmit final beacon.

# Requirement Allocation Sheet

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **ID** | **System Requirement** | **ID** | **Design Requirement** | **ID** | **Verification Requirement** | **Verification Method** |
| SR1 | Send the CW data | DR1.1 | Collect CW data from each sub system | VR1.1.1 | C&DH and other sub system is connected by UART | Check the data between OBC and other sub system |
| DR1.2 | Save the data | VR1.2.1 | OBC PIC save the data on memory | Check the saved the data on Flash memory |
| DR1.3 | Count the time | VR1.3.1 | OBC PIC count the time | Check the count data on OBC PIC |
| DR1.4 | Send these data to COM PIC | VR1.4.1 | Received the data on COM PIC | Check the data on COM PIC |
| SR2 | Collect and store HK data | DR2.1 | Collect HK data from each system | VR.2.1.1 | C&DH and Other Sub System is connected by UART | Check the data between OBC and other Sub Systems |
| DR2.2 | Save the data | VR.2.2.1 | OBC PIC save the data on memory | Check the saved the data on Flash memory |
| DR2.3 | Send these data to COM PIC | VR.2.3.1 | Received the data on COM PIC | Check the data on COM PIC |
| SR3 | Analyse uplink commands | DR3.1 | Get the uplink command from COM | VR3.1.1 | Received the data on OBC PIC | Check the data on OBC PIC |
| DR3.2 | Analyse the command | VR3.2.1 | Verify command data is accurate | Compare the uplink details and tested data during EM testing |
| DR3.3 | Send the command to each system | VR3.3.1 | Received the data on each system | Check Sub Systems |
| DR5.3 | Reset the satellite | VR5.3.1 | Send the command to Reset PIC | Check the data on Reset PIC |

# Schedule

|  |  |  |  |
| --- | --- | --- | --- |
| Milestone | Planned Date | Actual Date | Notes |
| Requirements Freeze | 20240926 | 20240926 |  |
| CDR (Critical Design Review) | 20241226 | 20241226 |  |
| Proto flight Board Fabrication | 20250126 | 20250126 |  |
| Flight Software V1.0 | 20250426 | 20250426 |  |
| Integration & Test | 20250626 | 20250626 |  |
| Delivery for Launch | 20250926 | 20250926 |  |