Configurable Backplane

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July 13, 2022

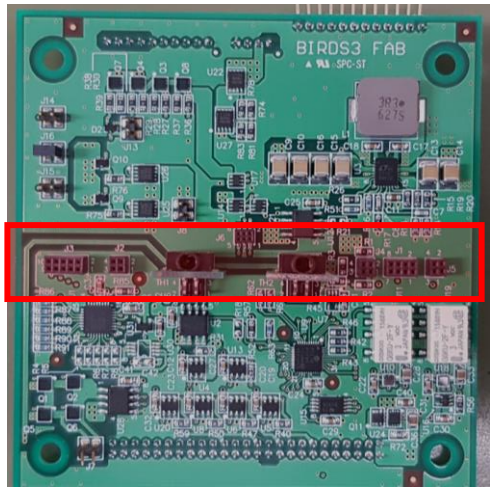
BIRDS Program

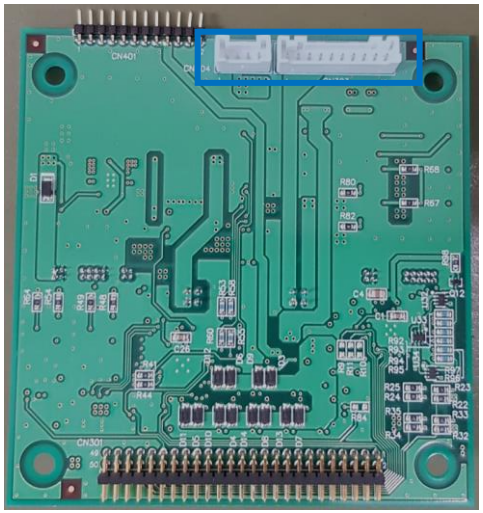
"successfully build, test, launch and operate satellite of non-space fairing countries"

BIRDS-1 (2015-2017)		Japan	Ghana*	Mongolia*	Nigeria	Bangladesh*
BIRDS-2 (2016-2018)		Japan	Philippines	Malaysia	Bhutan*	
BIRDS-3 (2017-2019)		Japan	Sri Lanka*	Nepal*		
BIRDS-4 (2018-2020)		Japan	Philippines	Paraguay*		
BIRDS-5 (2020-2022)		Japan	Uganda*	Zimbabwe*		

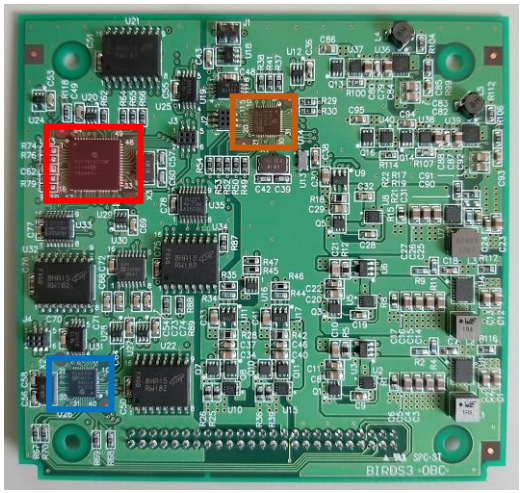
*country's first satellite

BIRDS 1U Standard Bus





Front Access Board



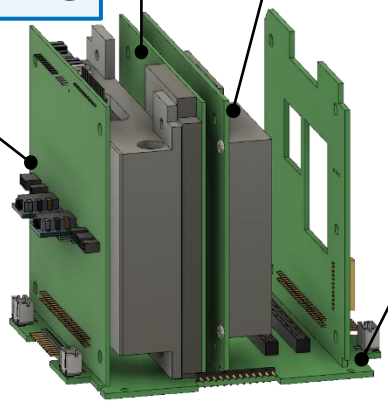
OBC/EPS

COM (UHF transceiver)

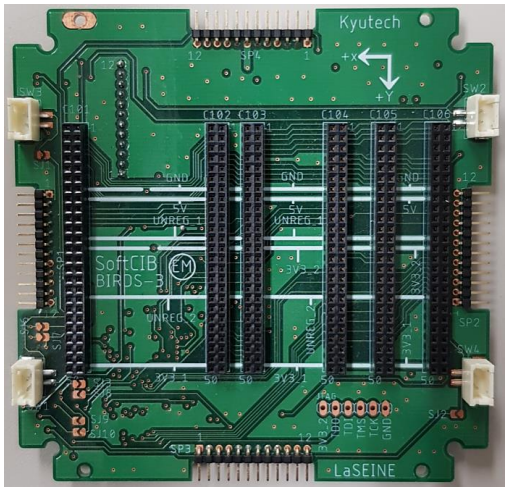
Main PIC

Reset PIC

COM PIC



BIRDS CubeSat internal view

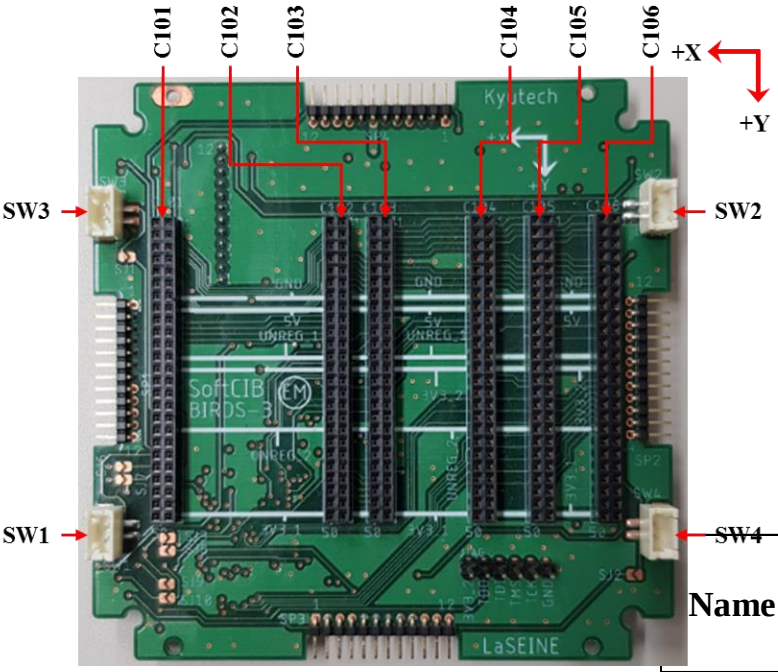


Backplane Board

Umbilical and Flight Pins

Battery connector

BIRDS 1U Backplane (1/2)



Backplane
Top side

Backplane provides electrical and mechanical interface between components satellite components.

Features

- Easy to assemble and disassemble
- Less use of harness
- Enough connector size and pin count

Name	No. of pins	Description	Manufacturer Model	Current rating [A]	Voltage rating [V]	Operating Temp [°C]
C101-C106	50	FAB, OBC/EPS, COM, MSN1 MSN2, RAB	Hirose A3C-50DA-2DSA (71)	1	200	-55 to +85
SW1-SW4	2	Dep. SW1 Dep. SW2 Dep. SW3 Dep. SW4	Molex 554600272	1.5	125	-40 to +105
SP1-SP4	12	+X solar panel +Y solar panel -Y solar panel Antenna panel	Hirosugi PSR-210154-12	1	500	-40 to +105
SP5	12	-Z Solar Panel	Hirosugi PSS-210204-12	1	500	-40 to +105

FAB: Front Access Board
OBC: On-Board Computer
EPS: Electric Power Subsystem
MSN: Mission
RAB: Rear Access Board
BPB: Backplane Board

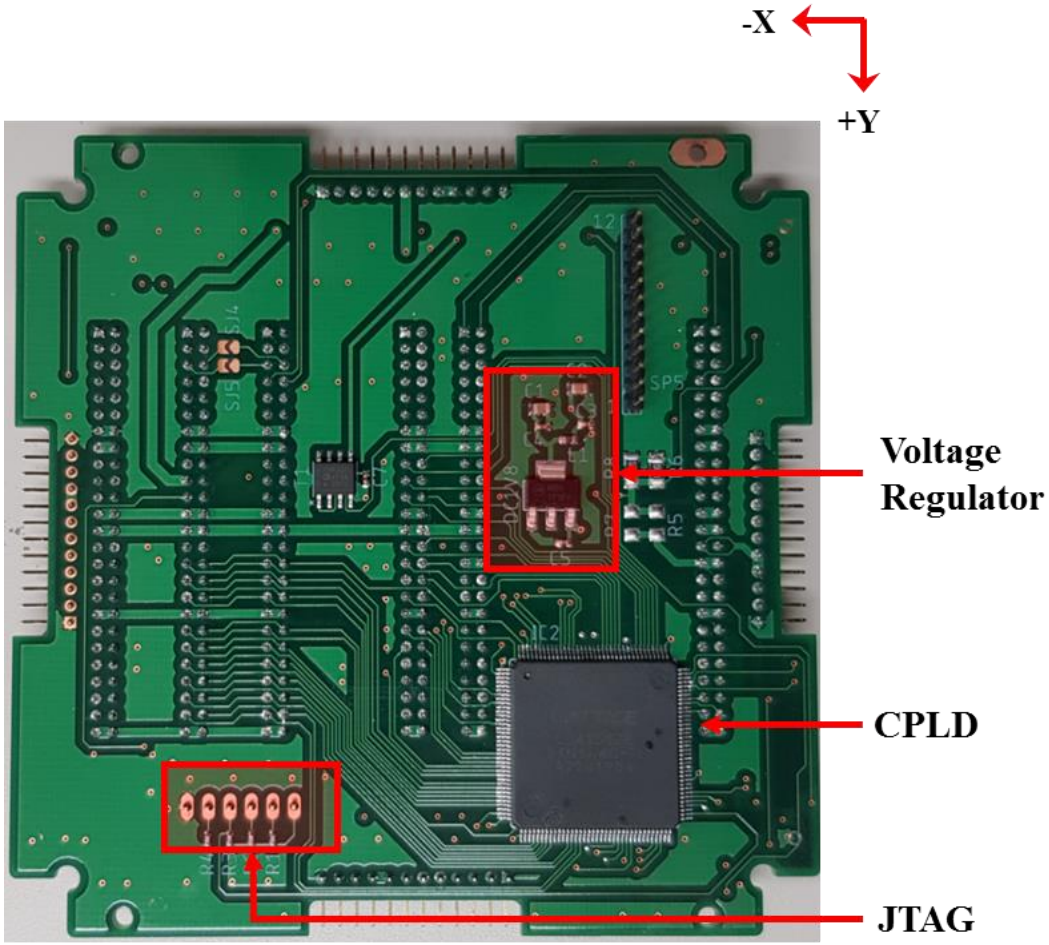
BIRDS 1U Backplane (1/2)

CPLD (Complex Programmable Logic Device)

- Flight-proven (BIRDS-3 heritage)
- Lattice Semiconductor 4256ZE
- Ultra-low power PLD (13uA standby current)
- 1.8V LVCMOS technology
- 20mm x 20mm QFP (quad-flat pack)
- JTAG for programming

Voltage Regulator

- Input: 3.3V; Output: 1.8V
- 4.2mA quiescent current



Backplane
Bottom side

CPLD Implementation (1/2)

Digital lines between the bus (OBC/EPS) and the mission payload are routed through CPLD

- 11 pins as (DIO, UART)
- 4 pins (SPI)

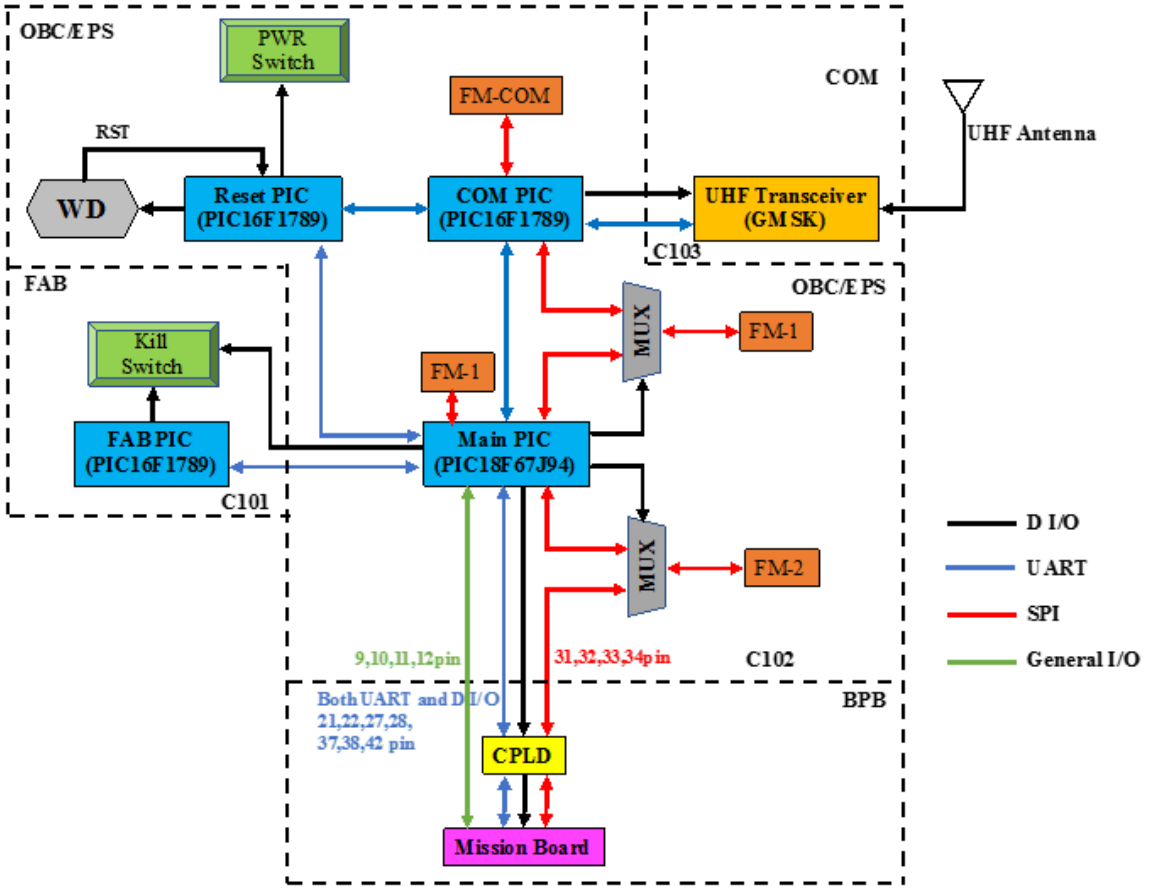


Figure 4.4 Data transfer between platform and payload

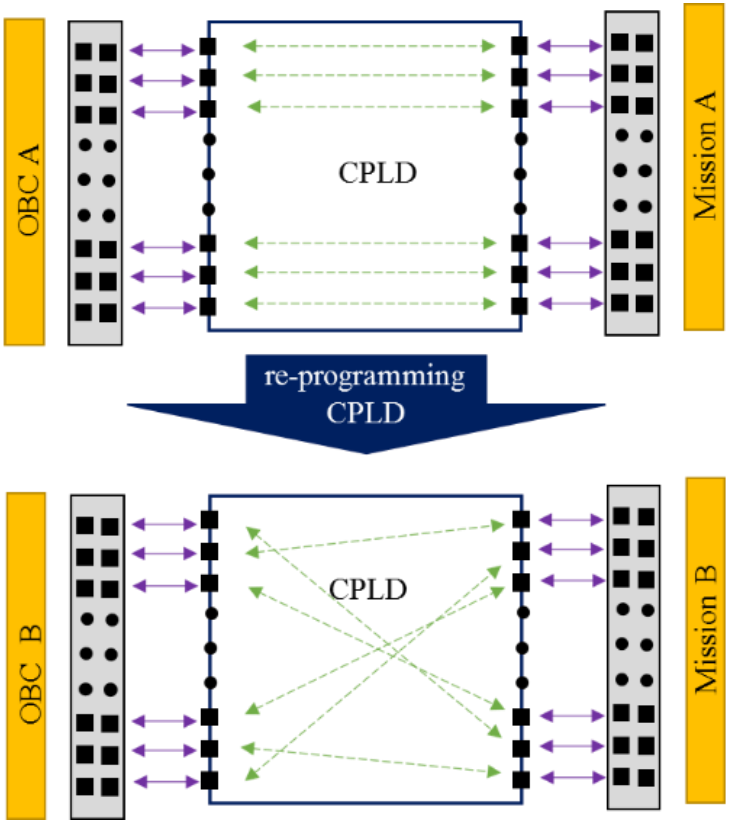
C102 (OBC/EPS)			
Signal Name	Pin Number		Signal Name
Prog_GIO_1	1	2	Prog_GIO_2
Prog_GIO_3	3	4	Prog_GIO_4
Prog_GIO_5	5	6	Prog_GIO_6
OBC-COM_1	7	8	OBC-COM_2
FAB_to_RAB_GIO_3	9	10	FAB_to_RAB_GIO_4
FAB_to_RAB_GIO_5	11	12	FAB_to_RAB_GIO_6
GND-SYS	13	14	GND-SYS
SUP_5V0	15	16	SUP_5V0
FAB_to_OBC_GIO_1	17	18	FAB_to_OBC_GIO_2
FAB_to_OBC_GIO_3	19	20	FAB_to_OBC_GIO_4
CPLD8	21	22	CPLD9
SUP_UNREG_1	23	24	SUP_UNREG_1
SUP_3V3_2	25	26	SUP_3V3_2
CPLD10	27	28	CPLD11
RAW_POWER	29	30	RAW_POWER
CPLD12	31	32	CPLD13
CPLD14	33	34	CPLD15
SUP_UNREG_2	35	36	SUP_UNREG_2
CPLD16	37	38	CPLD17
Kill_SW	39	40	DEP_SW_1
DEP_SW_2	41	42	CPLD18
OBC-COM_3	43	44	OBC-COM_4
OBC-COM_5	45	46	OBC-COM_6
OBC-COM_7	47	48	OBC-COM_8
SUP_3V3_1	49	50	SUP_3V3_1

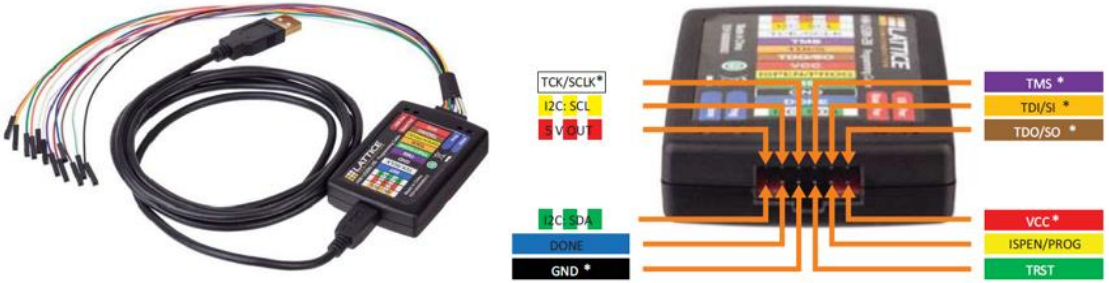
OBC/EPS pin assignment

CPLD Implementation (2/2)

CPLD configures the communication between the bus and the mission payload by software

- VHDL or Verilog code
- Lattice **ispLEVER Classic** IDE (Student license available)
  https://www.latticesemi.com/ispleverclassic
- **Lattice Diamond Programmer** to load JEDEC file to the CPLD (free)
  https://www.latticesemi.com/Products/DesignSoftwareAndIP/ProgrammingAndConfigurationSw/Programmer
- CPLD programming cable is needed to program CPLD
  https://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/Program





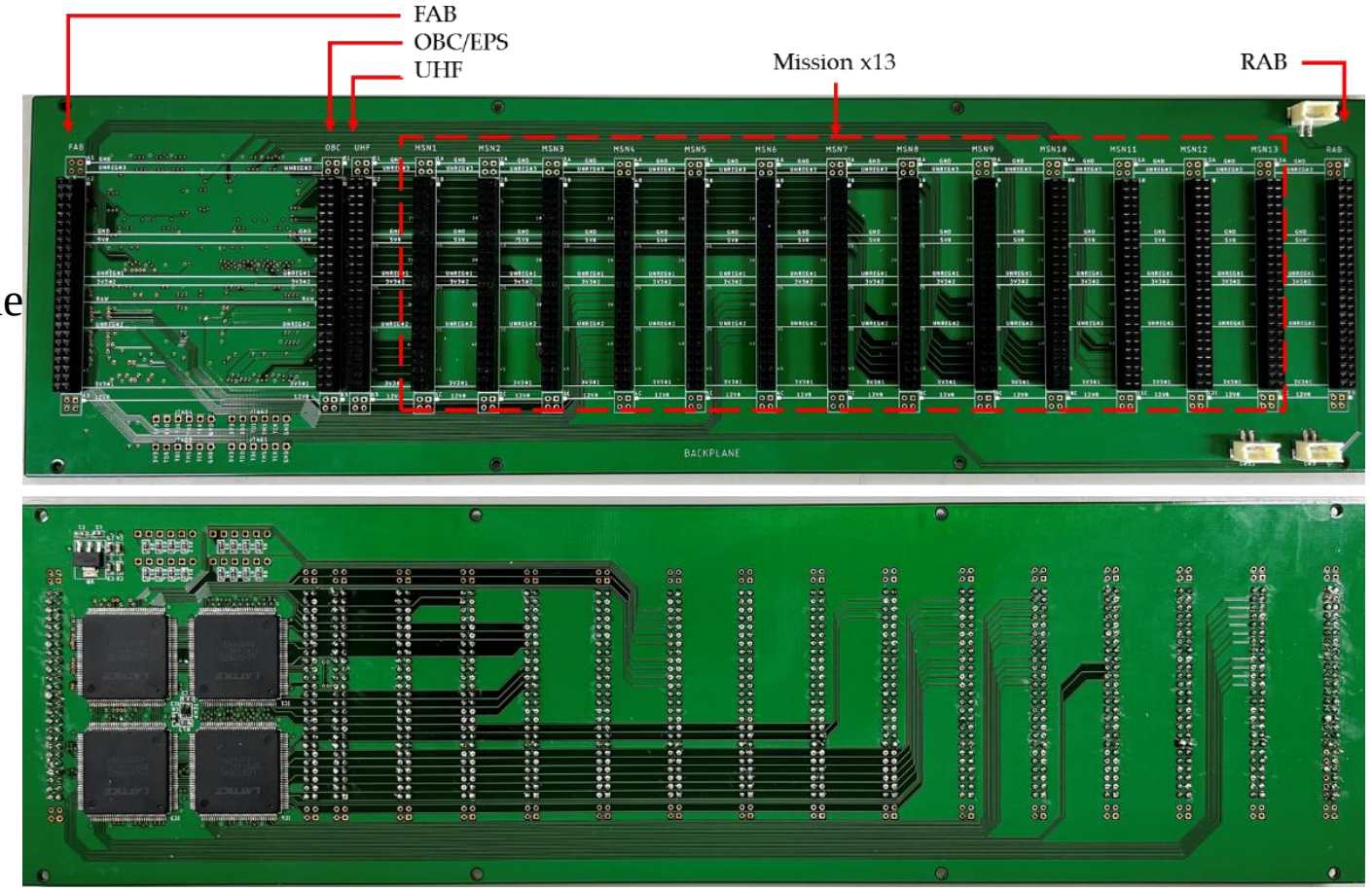
Lattice HW-USBN-2B programming cable

Case study 1: BIRDS bus in 3U

- BIRDS bus was designed to be scalable in larger CubeSat platforms, with minimal modifications
- Requirements - BIRDS 1U bus architecture is kept; maximize backplane space for missions

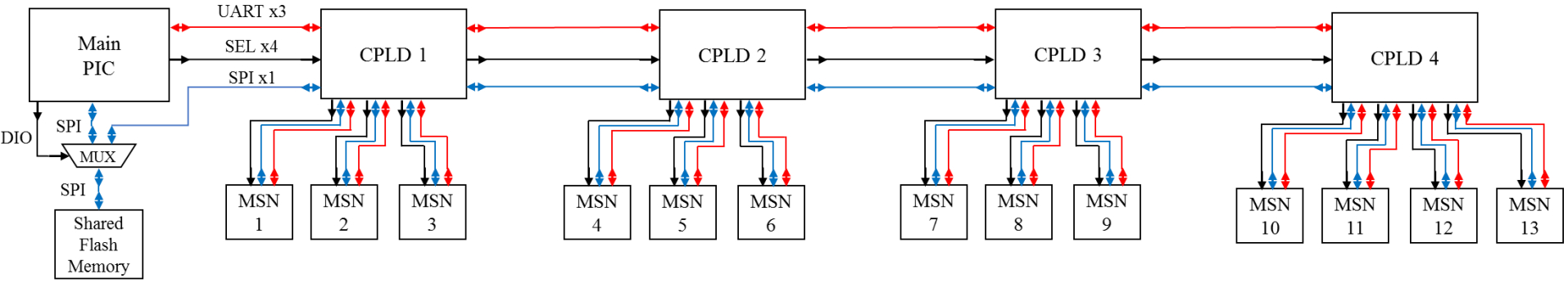
3U configurable backplane

- 320 x 90 x 1.6 mm
- 6-layer PCB
- 13 mission boards
- 4 CPLDs
- 1 voltage regulator



Case study 1: BIRDS bus in 3U

- **Constraint** – digital lines available in OBC/EPS
- **Solution** – CPLDs as MUX



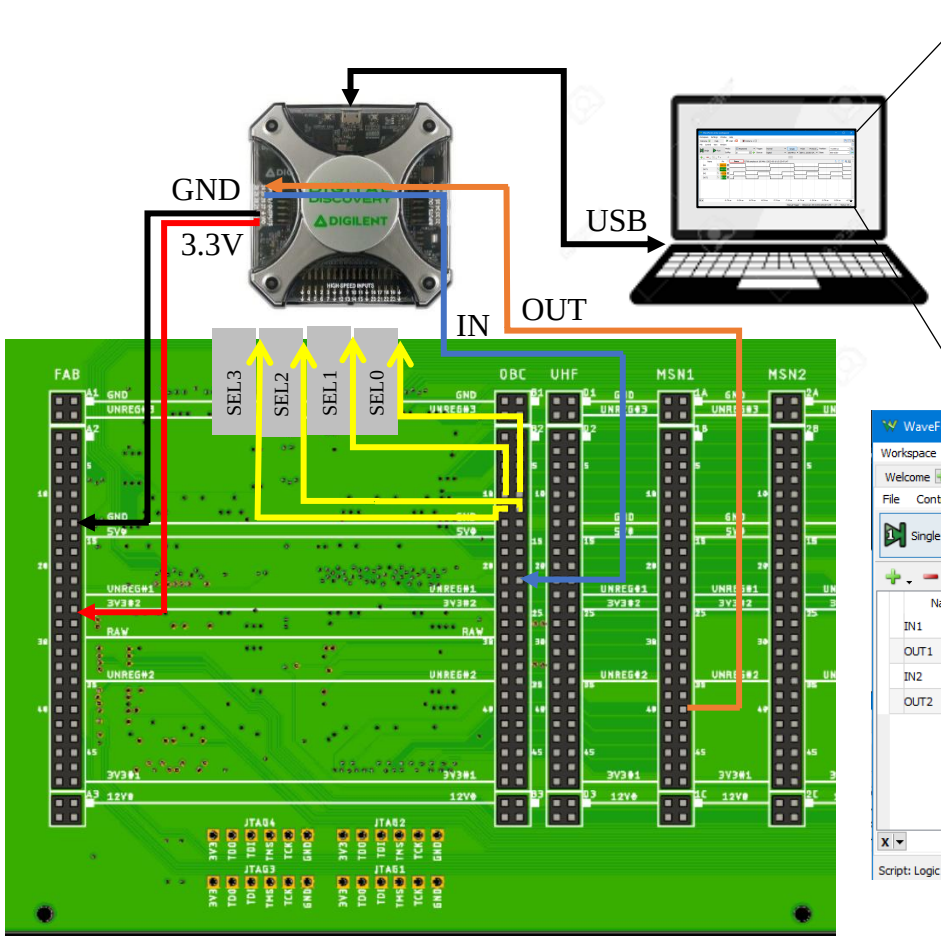
Truth Table

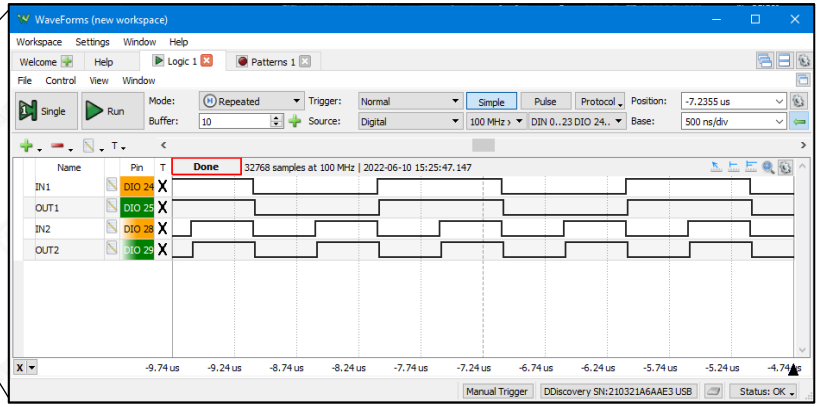
Input				Output			
Select 3	Select 2	Select 1	Select 0	CPLD 1	CPLD 2	CPLD 3	CPLD 4
0	0	0	1	MSN 1	-	-	-
0	0	1	0	MSN 2	-	-	-
0	0	1	1	MSN 3	-	-	-
0	1	0	0	CPLD 2	MSN 4	-	-
0	1	0	1	CPLD 2	MSN 5	-	-
0	1	1	0	CPLD 2	MSN 6	-	-
0	1	1	1	CPLD 2	MSN 7	MSN 7	-
1	0	0	0	CPLD 2	MSN 8	MSN 8	-
1	0	0	1	CPLD 2	CPLD 3	MSN 9	-
1	0	1	0	CPLD 2	CPLD 3	CPLD4	MSN 10
1	0	1	1	CPLD 2	CPLD 3	CPLD4	MSN 11
1	1	0	0	CPLD 2	CPLD 3	CPLD4	MSN 12
1	1	0	1	CPLD 2	CPLD 3	CPLD4	MSN 13

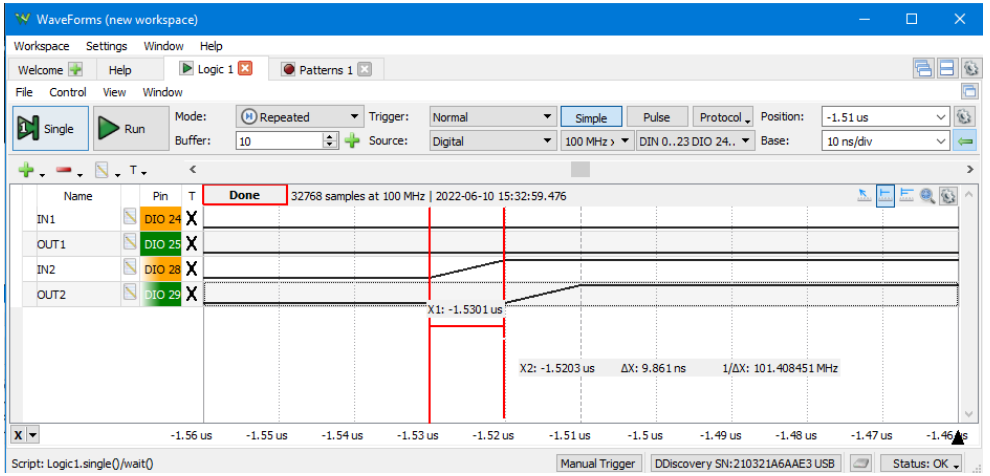
```
port(
    CP_IN: in std_logic_vector ( 27 downto 0 );
    CP_OUT: out std_logic_vector ( 21 downto 0 );
    SEL_IN: in std_logic_vector ( 3 downto 0 );
    SEL_OUT: out std_logic_vector ( 3 downto 0 ) );

end entity cpld1;

architecture cpld1 of cpld1 is
begin

process (SEL_IN, CP_IN) is
begin
    if(SEL_IN(0)='1' and SEL_IN(1)='0' and SEL_IN(2)='0' and SEL_IN(3)='0') then
        CP_OUT(6) <= CP_IN(0);          -- UART1(MAIN2MSN); pin21 -> pin68
        CP_OUT(0) <= CP_IN(4);          -- UART1(MSN2MAIN); pin67 -> pin22
        CP_OUT(7) <= CP_IN(1);          -- UART2(MAIN2MSN); pin5 -> pin53
        CP_OUT(1) <= CP_IN(5);          -- UART2(MAIN2MSN); pin52 -> pin4
        CP_OUT(8) <= CP_IN(2);          -- UART3(MAIN2MSN); pin25 -> pin42
        CP_OUT(2) <= CP_IN(6);          -- UART3(MAIN2MSN); pin43 -> pin26
        CP_OUT(3) <= CP_IN(7);          -- SPI_CS(MSN2SFM); pin88 -> pin11
        CP_OUT(9) <= CP_IN(3);          -- SPI_MISO(SFM2MSN); pin12 -> pin101
        CP_OUT(4) <= CP_IN(8);          -- SPI_MOSI(MSN2SFM); pin87 -> pin13
        CP_OUT(5) <= CP_IN(9);          -- SPI_CLK(MSN2SFM); pin100 -> pin14
```

All 4 CPLDs where programmed based on truth table.

Functional test

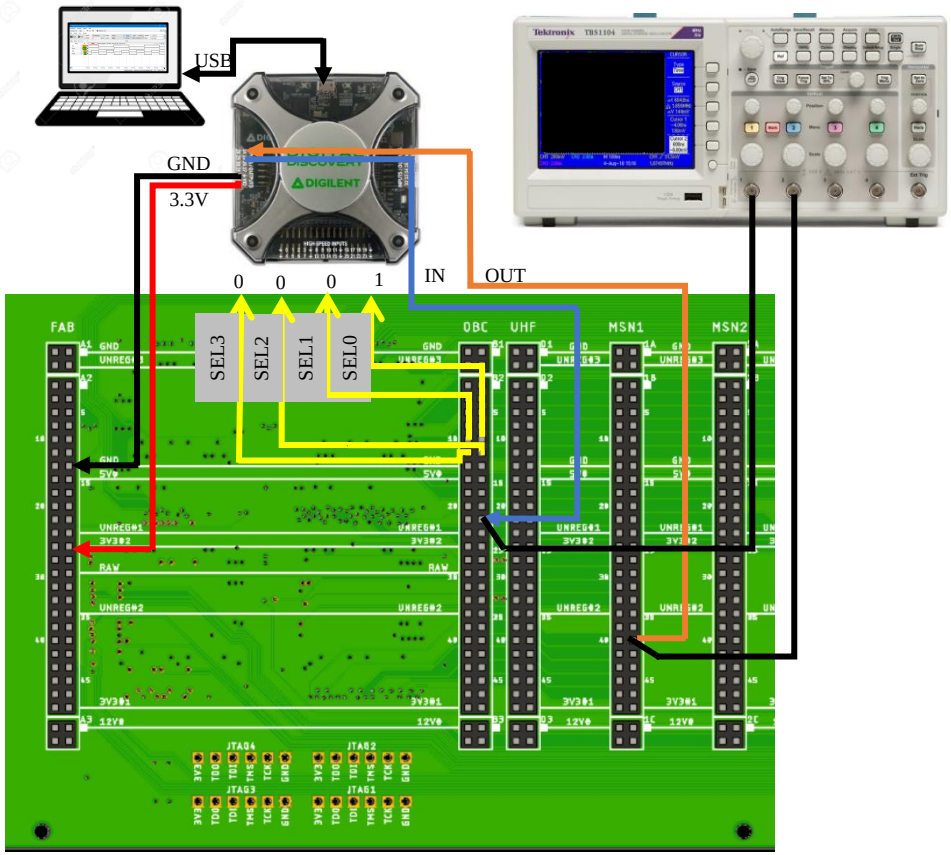




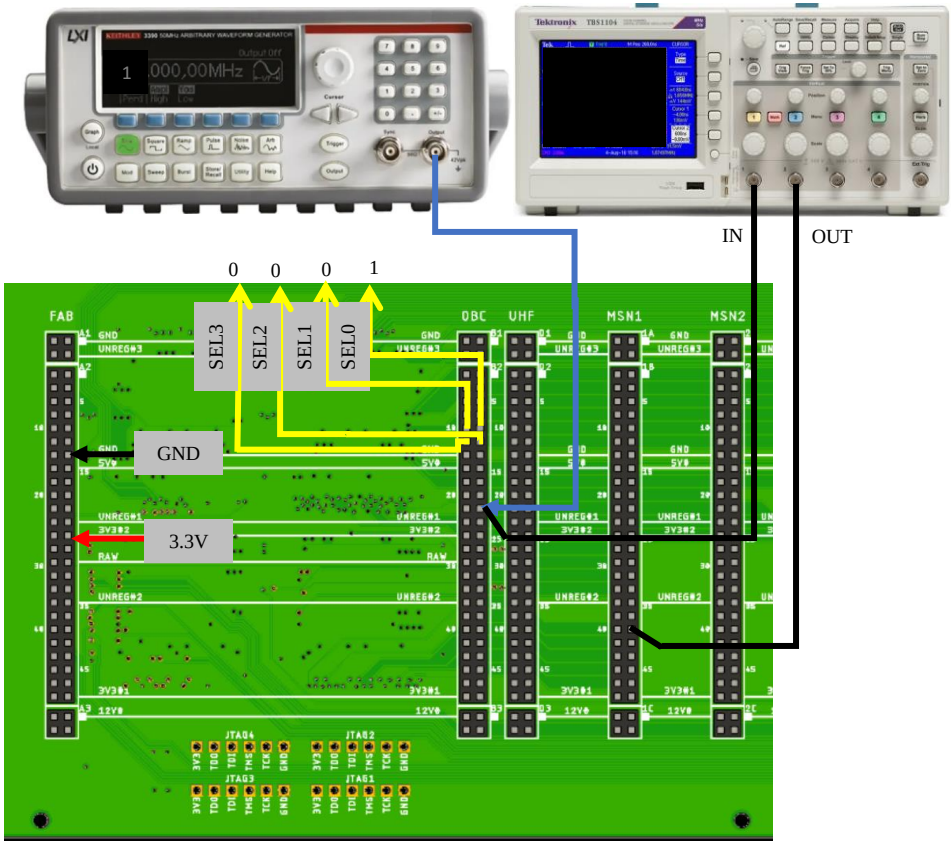


Propagation delay (1 CPLD) is 9.86ns.
Need more accurate measurements

Propagation delay measurement (1/2)

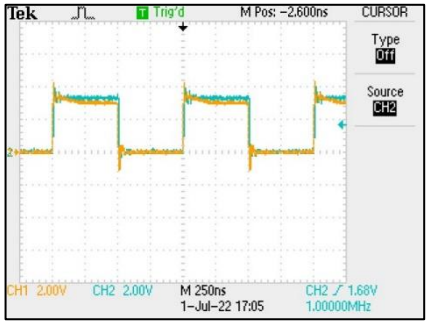


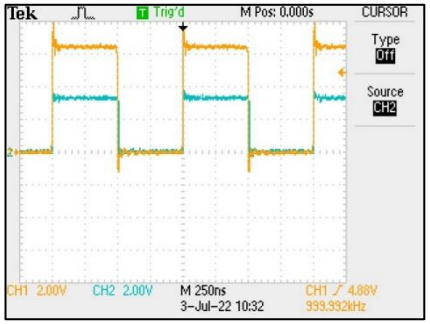
Setup 1: logic analyzer + oscilloscope

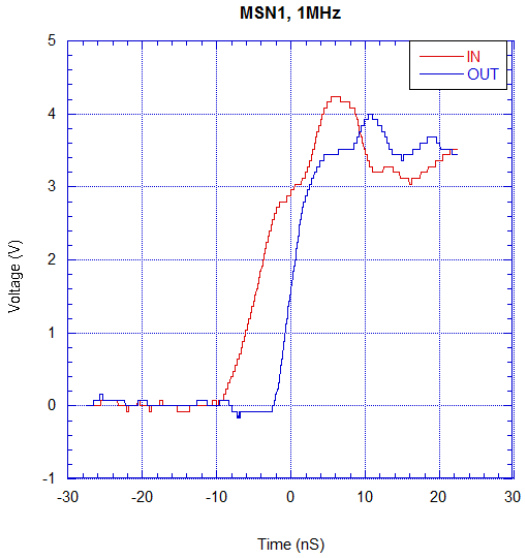


Setup 2: function generator + oscilloscope

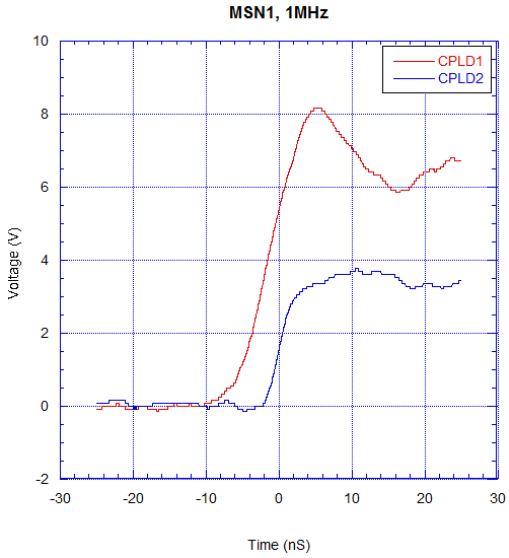
Propagation delay measurement (2/2)







Setup 1: logic analyzer + oscilloscope

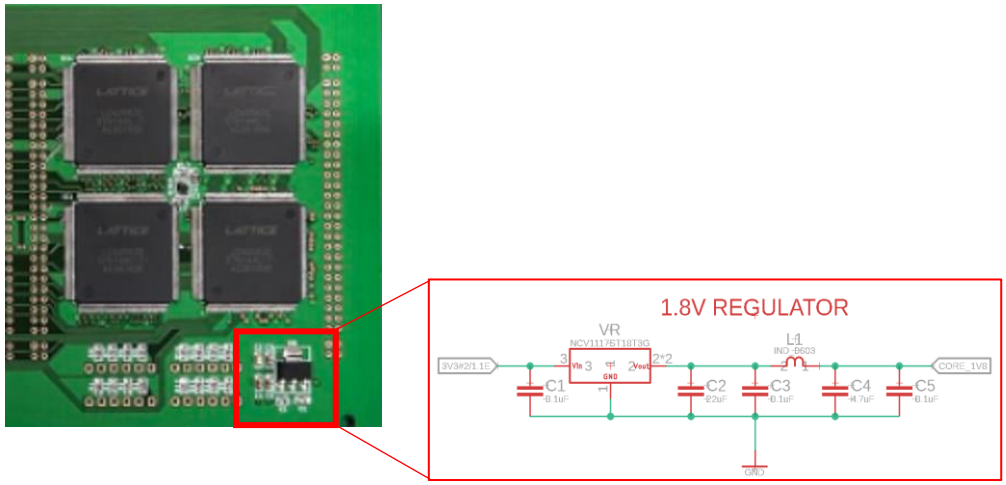


Setup 2: function generator + oscilloscope

- Input: 1MHz square wave, 3.3Vpp
- Measurements were also done using 25 MHz square wave input. No significant difference in propagation delay.
- Because of impedance mismatch, the signal from function generator appears twice the magnitude in the oscilloscope (Setup2).
- From the datasheet, LC4256ZE-5TNI has max propagation delay of 5.8ns
- Results show that propagation delay is cumulative delays of all CPLDs
- Output voltage is not degraded as signal passes CPLDs

	Propagation delay	
	Setup 1	**Setup 2**
CPLD1	5.2 ns	6.0 ns
CPLD1-2	9.4 ns	10.2 ns
CPLD1-3	13.3 ns	14.0 ns
CPLD1-4	18.5 ns	16.8 ns

Power measurement



Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Current	I_Q				mA
1.5 V (V_{in} = 11.5 V)		–	3.6	10	
1.8 V (V_{in} = 11.8 V)		–	4.2	10	
1.9 V (V_{in} = 11.9 V)		–	4.3	10	
2.0 V (V_{in} = 12 V)		–	4.5	10	
2.5 V (V_{in} = 10 V)		–	5.2	10	
2.85 V (V_{in} = 10 V)		–	5.5	10	
3.3 V (V_{in} = 15 V)		–	6.0	10	
5.0 V (V_{in} = 15 V)		–	6.0	10	
12 V (V_{in} = 20 V)		–	6.0	10	

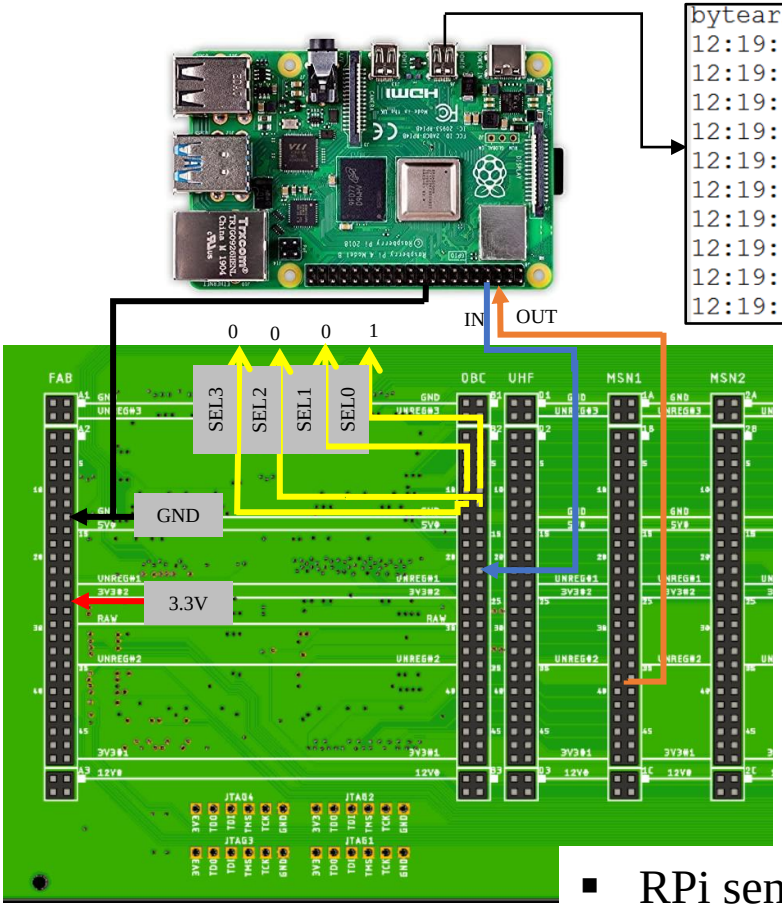
ispMACH 4256ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8 V, T_A = 25 °C	—	341	—	µA
		Vcc = 1.9 V, T_A = 0 to 70 °C	—	361	—	µA
		Vcc = 1.9 V, T_A = –40 to 85 °C	—	372	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8 V, T_A = 25 °C	—	13	—	µA
		Vcc = 1.9 V, T_A = 0 to 70 °C	—	32	65	µA
		Vcc = 1.9 V, T_A = –40 to 85 °C	—	43	100	µA

1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6 V, V_{IN} = 0 V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15 µA typical current plus additional current from any logic it drives.

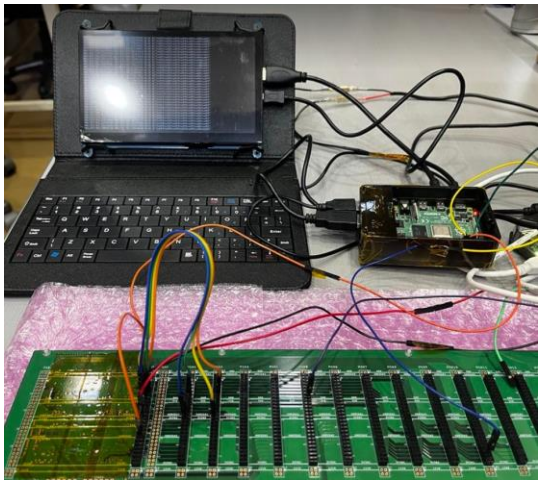
- 1 voltage regulator for all four CPLDs
- From datasheet, voltage regulator (NCV1117ST18T3G) quiescent current is 4.2mA. This is verified in a test.
- From datasheet, CPLD (4256ZE)
  - standby current is 13uA
  - operating current is 341uA
- **Power consumption (idle):**
- **14.4 mW** (4mA, 3.3V)
- **Power consumption* (working): 17.7 mW** (5.4mA, 3.3V)

*all four CPLDs are ON

Bit error check

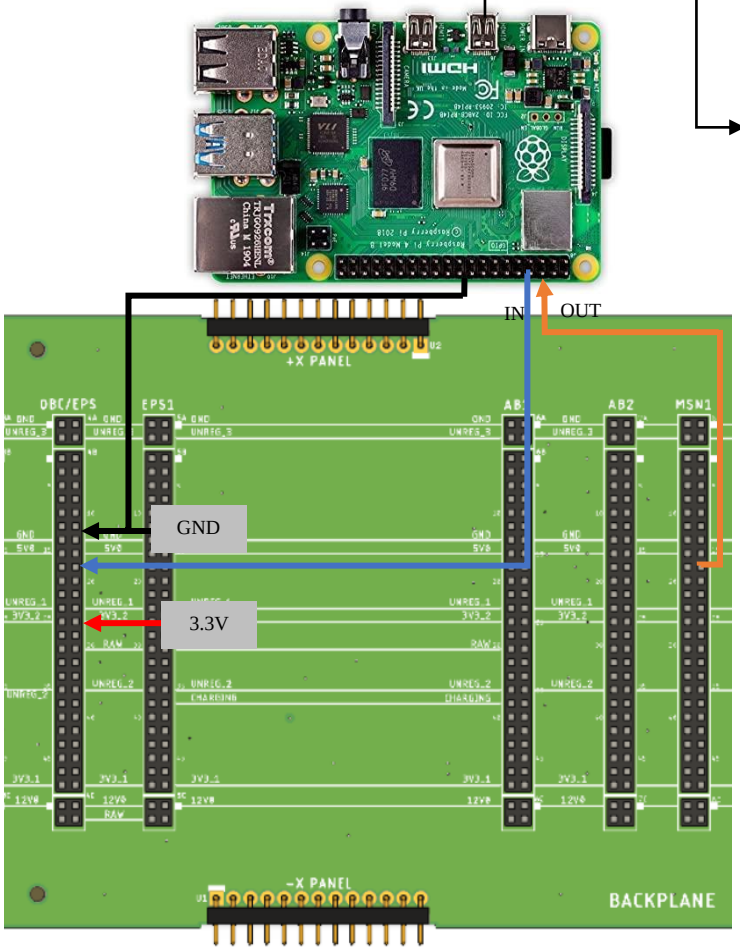



```
bytearray(b'\x00\x01\x02\x03\x04\x05\x06\x07')
12:19:15.394864 12:19:15.395621 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:15.697282 12:19:15.697526 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:15.998861 12:19:15.999091 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:16.300404 12:19:16.300624 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:16.601865 12:19:16.602078 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:16.903352 12:19:16.903581 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:17.204892 12:19:17.205106 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:17.506355 12:19:17.506566 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:17.807822 12:19:17.808029 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:18.109258 12:19:18.109471 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
```



- RPi sends 7 bytes of data (every 0.5 seconds) which passes through the CPLDs
- RPi receives the data from output pin of the last CPLD and compares it with the sent data
- Baud rate was varied from 1Mbps to 4Mbps.
- No bit errors recorded in the entire 5 minutes duration

Bit error check in thermal vacuum




```
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12:19:15.697282 12:19:15.697526 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:15.998861 12:19:15.999091 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:16.300404 12:19:16.300624 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:16.601865 12:19:16.602078 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:16.903352 12:19:16.903581 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:17.204892 12:19:17.205106 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:17.506355 12:19:17.506566 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:17.807822 12:19:17.808029 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
12:19:18.109258 12:19:18.109471 0.0 b'\x01\x02\x03\x04\x05\x06\x07'
```
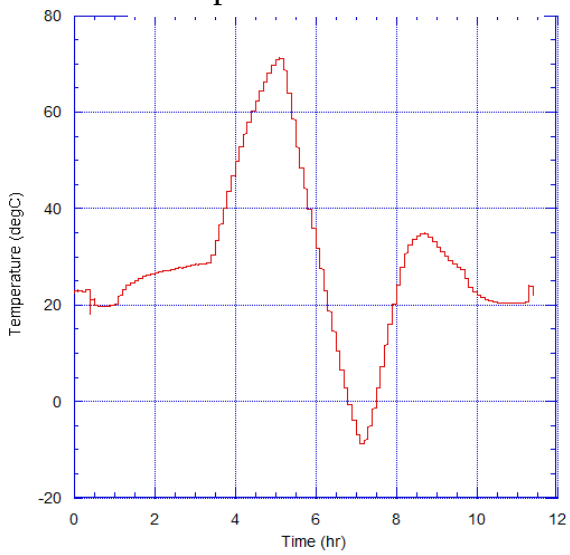

Temperature Profile

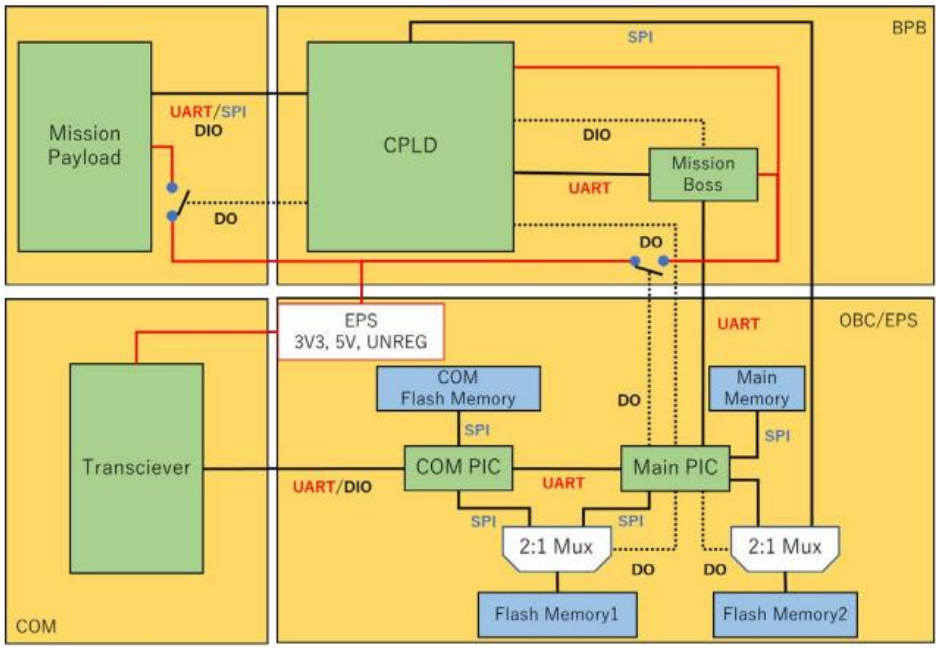


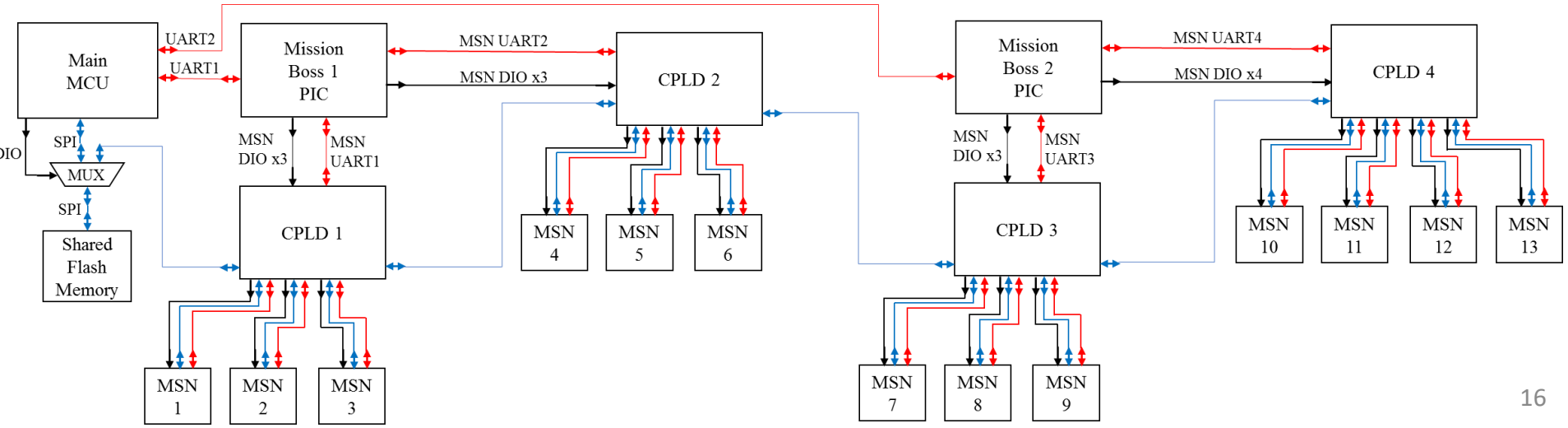
- RPi sends 7 bytes of data (every 0.5 seconds) which passes through the CPLD
- RPi receives the data from the output pin of CPLD and compares it with the sent data
- Baud rate was fixed to 1Mbps.
- Temperature: -10degC to +70degC
- No bit errors recorded in the entire 10 hours duration

Alternative Design

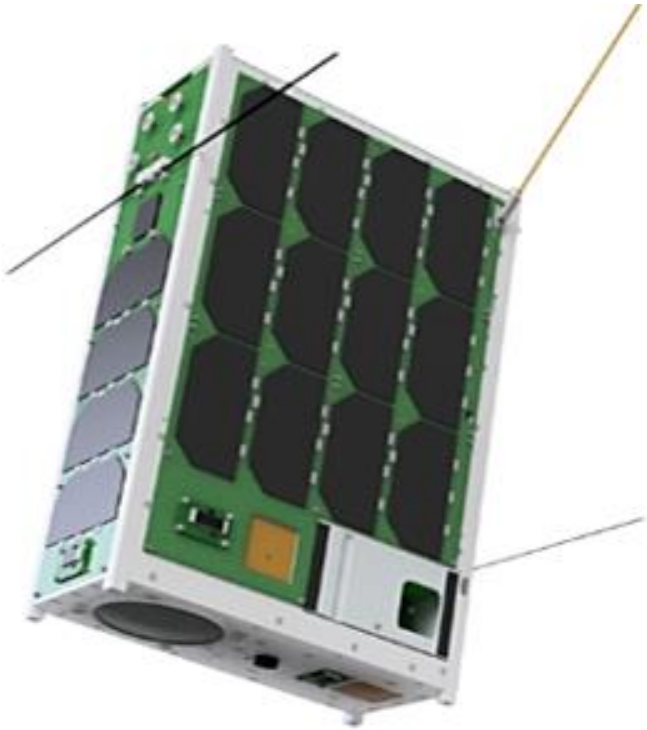
- Additional MCU (Mission Boss PIC) that directly communicates with Mission PIC
- Implemented in BIRDS-5 1U satellites

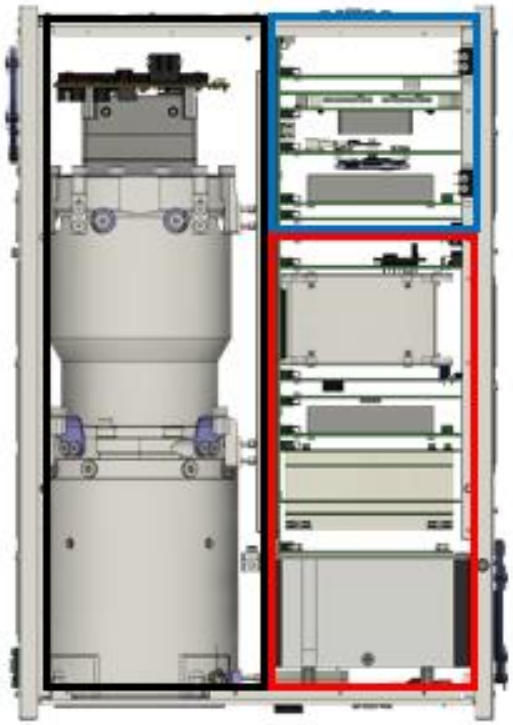
BIRDS-5 Design

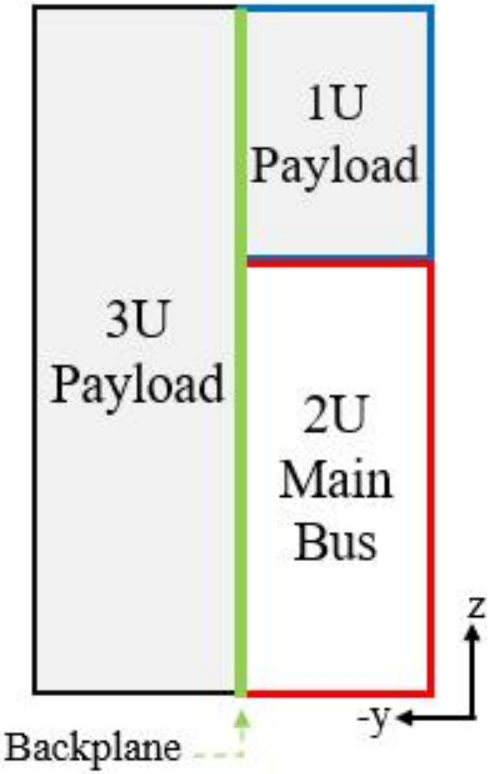




Case Study 2: KITSUNE W6U CubeSat





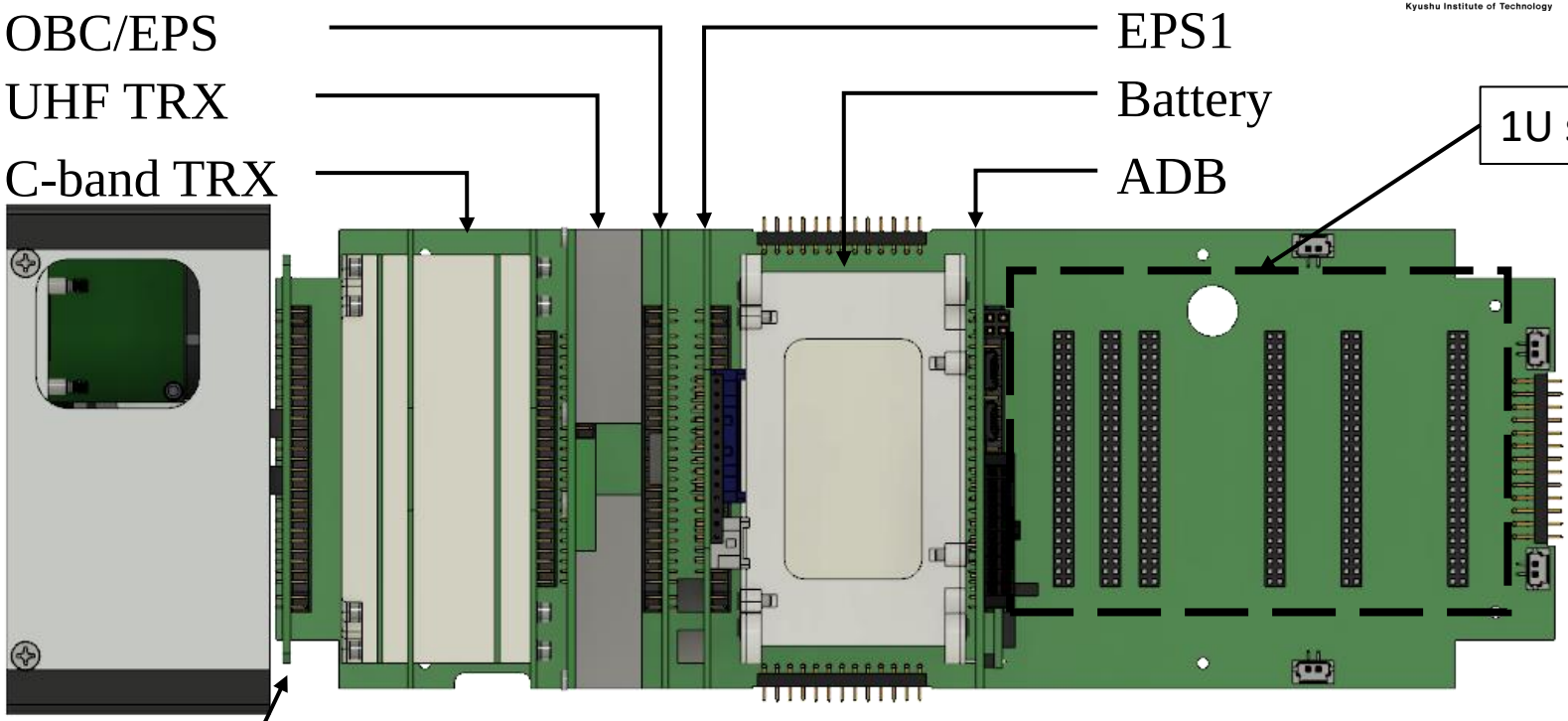


- Divided into 3 sections
- Sections are inter-connected through backplane

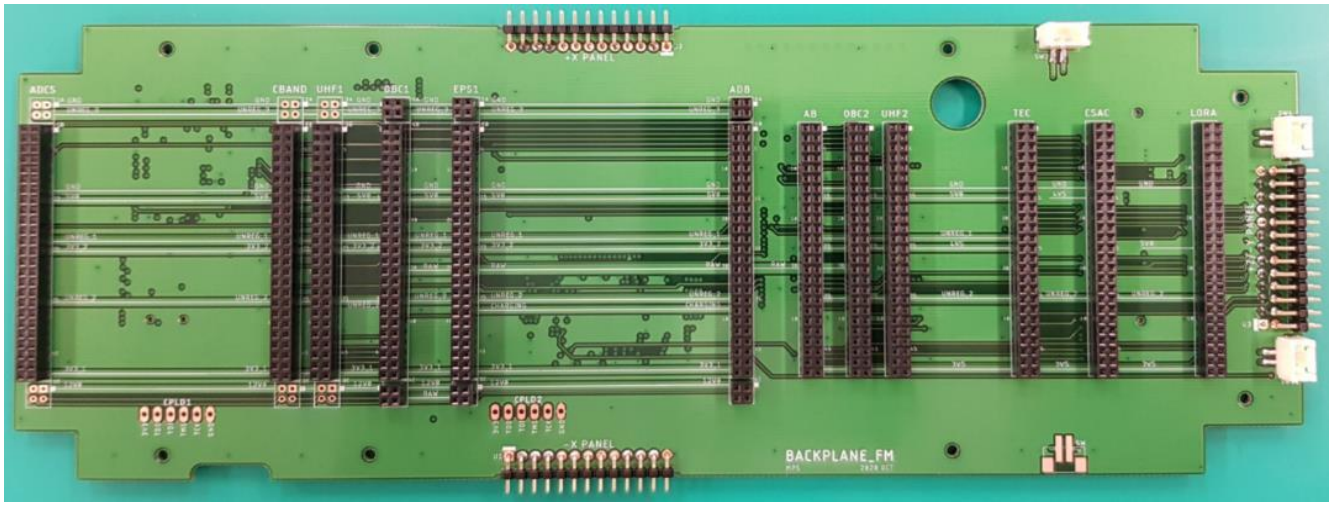
Bus Modifications

Board	BIRDS 1U bus	KITSUNE Main bus
FAB	Manages generated power, battery, electrical power safety, and umbilical	- Introduced a separate board (ADB) for umbilical - Power related functions are in EPS1 board
OBC/EPS	Command and data handling, and power distribution	- Additional power lines (12V, unregulated) and ground
Transceiver (TRX)	UHF	UHF + C-band
ADCS	None	With

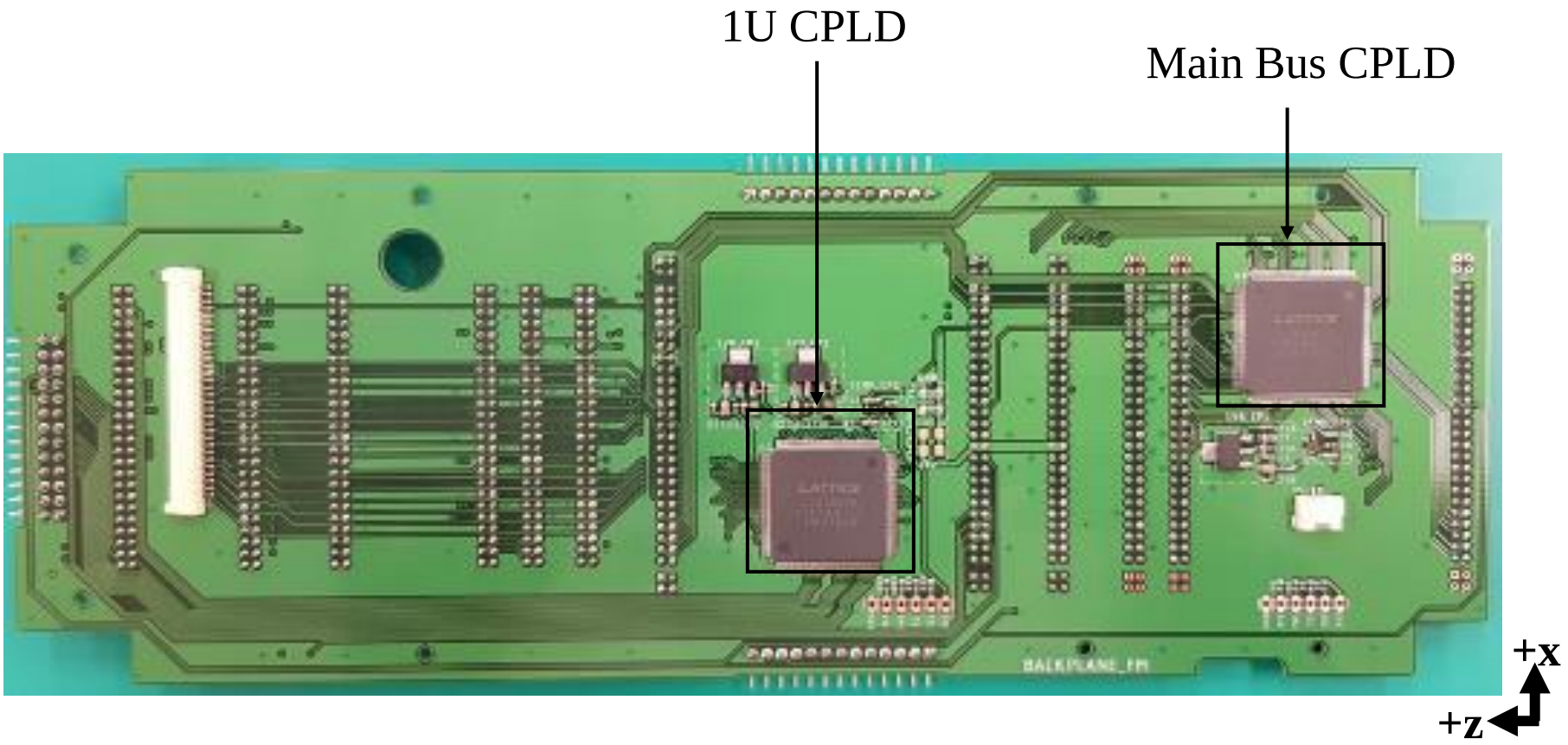
Backplane (Top)



ADCS Adapter board

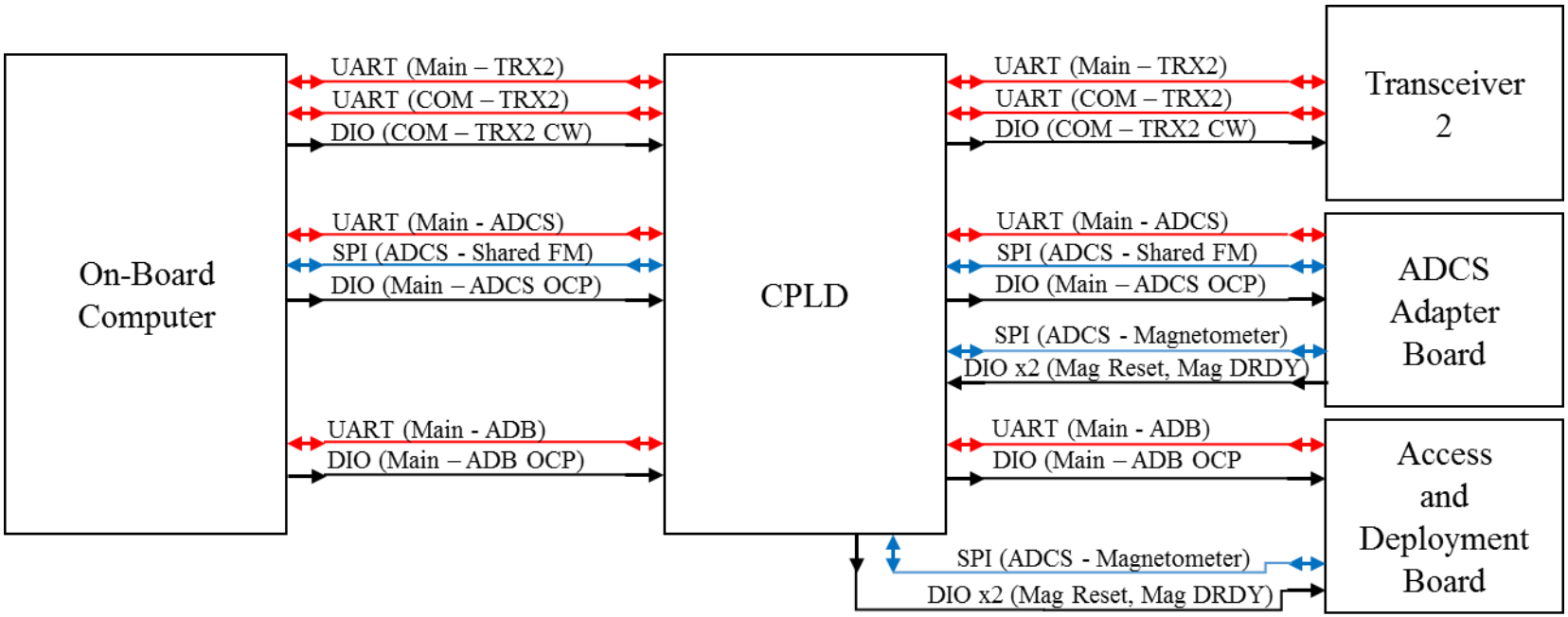


Backplane (Bottom)



- Two CPLDs (ispMACH4256E) were used for routing digital lines between boards

CPLD route configuration on Main Bus

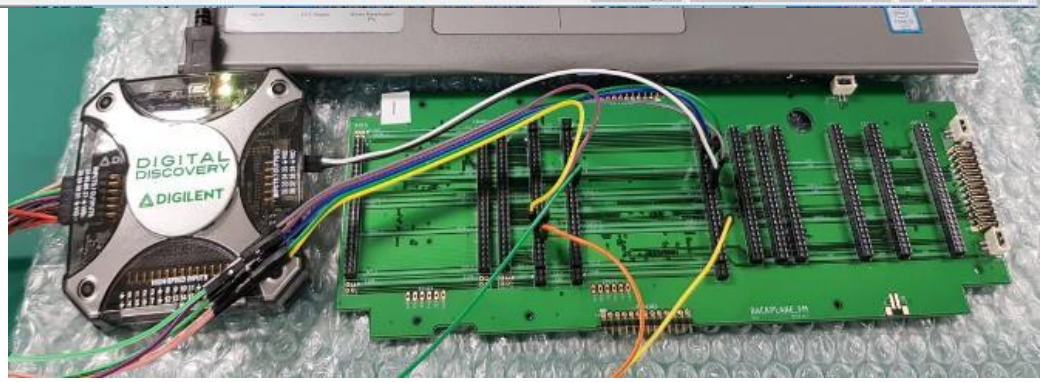


- 21 digital lines were routed using CPLD: 8 – UART, 8 – SPI, 5 – DIOs
- 45% of CPLD pins are utilized

Verification Results

- All 21 digital lines were verified to be working on both EM and FM boards
- Power consumption:
  13 mW

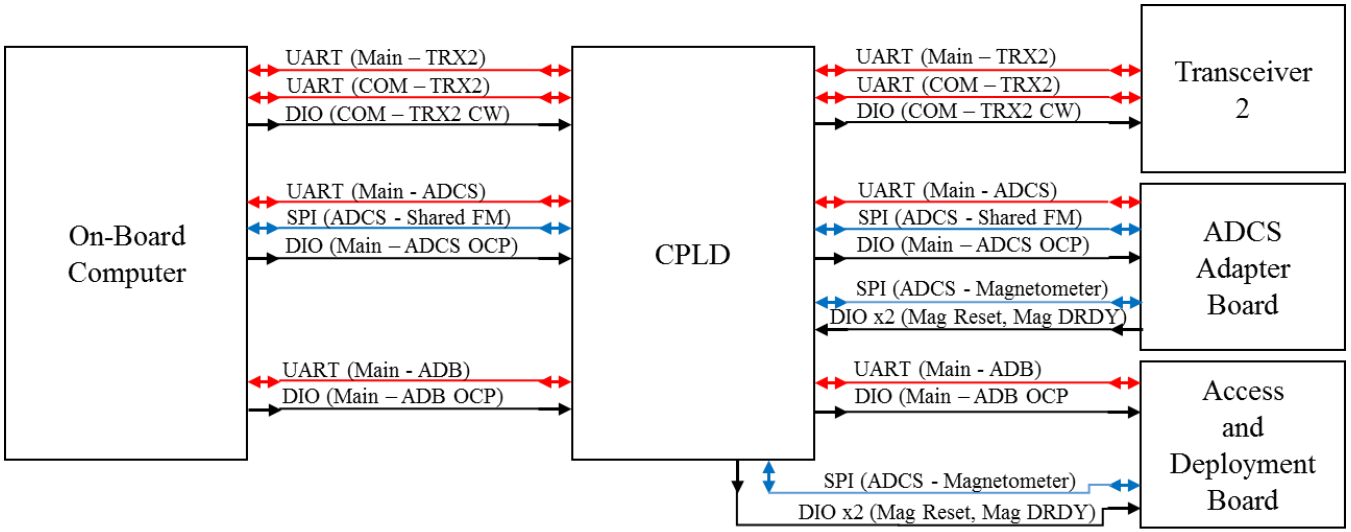
Digital lines	Baud rate	EM	FM
UART x2 (Main MCU – ADB MCU)	9,600	O	O
UART x2 (Main MCU – ADCS MCU)	9,600	O	O
UART x2 (Main MCU – TRX2)	115,200	O	O
UART x2 (COM MCU – TRX2)	115,200	O	O
SPI x4 (ADCS MCU – Magnetometer)	1,000,000	O	O
SPI x4 (ADCS MCU – Shared FM)	1,000,000	O	O
DIO (Main MCU – ADB OCP)	-	O	O
DIO (ADCS MCU – Magnetometer reset)	-	O	O
DIO (ADCS MCU –Magnetometer DRDY)	-	O	O
DIO (Main MCU – ADCS OCP)	-	O	O
DIO (COM MCU to TRX2 CW)	-	O	O



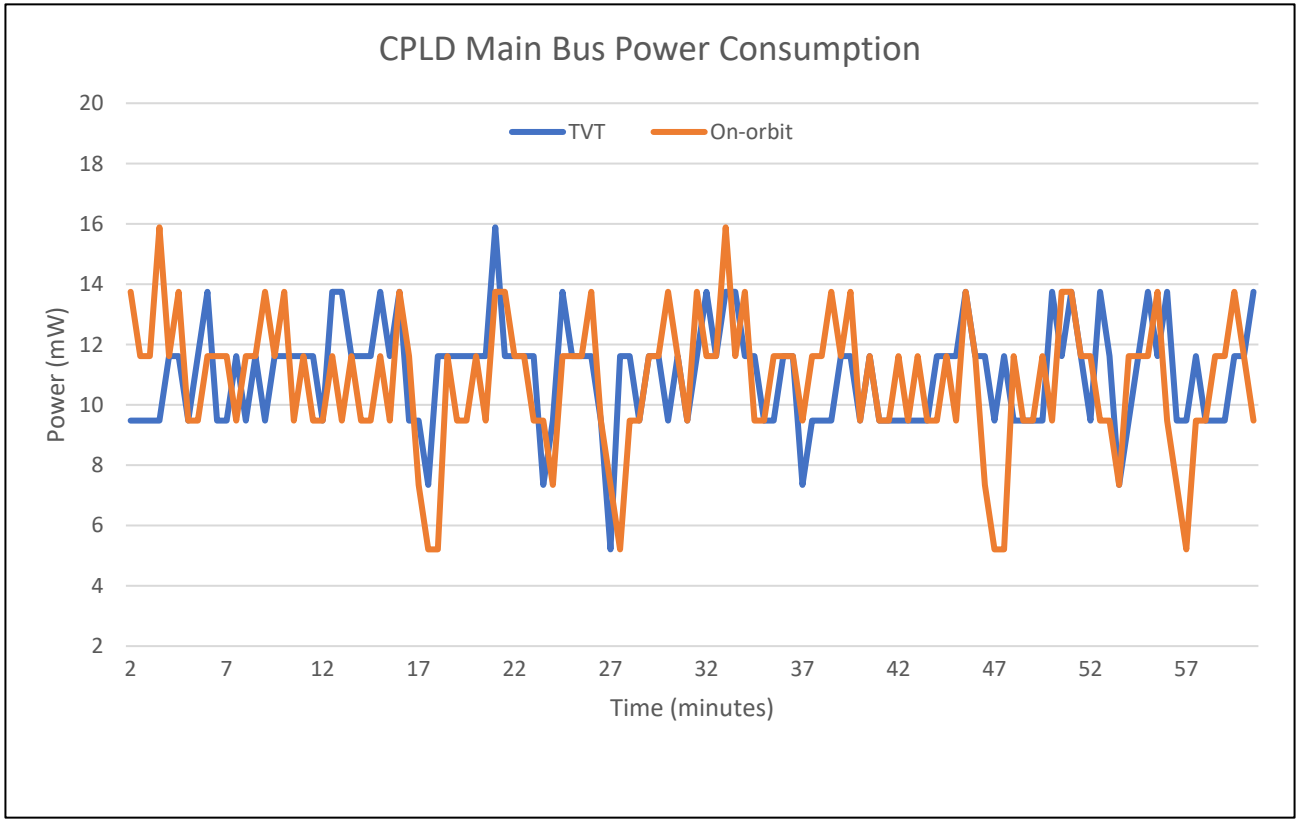
On-orbit Results (1/3)

All 21 digital lines were verified to be working with successful uplink and downlink

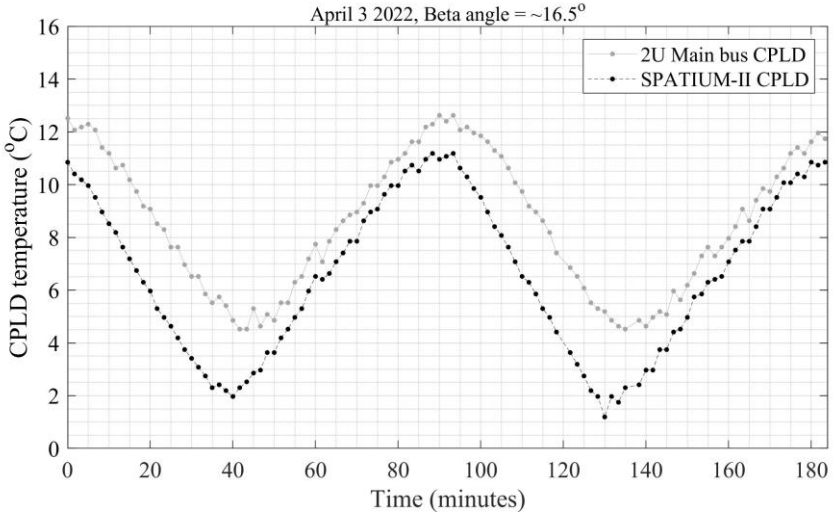
Digital lines	Baud rate	EM	FM	On-Orbit
UART x2 (Main MCU – ADB MCU)	9,600	○	○	○
UART x2 (Main MCU – ADCS MCU)	9,600	○	○	○
UART x2 (Main MCU – TRX2)	115,200	○	○	○
UART x2 (COM MCU – TRX2)	115,200	○	○	○
SPI x4 (ADCS MCU – Magnetometer)	1,000,000	○	○	○
SPI x4 (ADCS MCU – Shared FM)	1,000,000	○	○	○
DIO (Main MCU – ADB OCP)	-	○	○	○
DIO (ADCS MCU – Magnetometer reset)	-	○	○	○
DIO (ADCS MCU –Magnetometer DRDY)	-	○	○	○
DIO (Main MCU – ADCS OCP)	-	○	○	○
DIO (COM MCU to TRX2 CW)	-	○	○	○

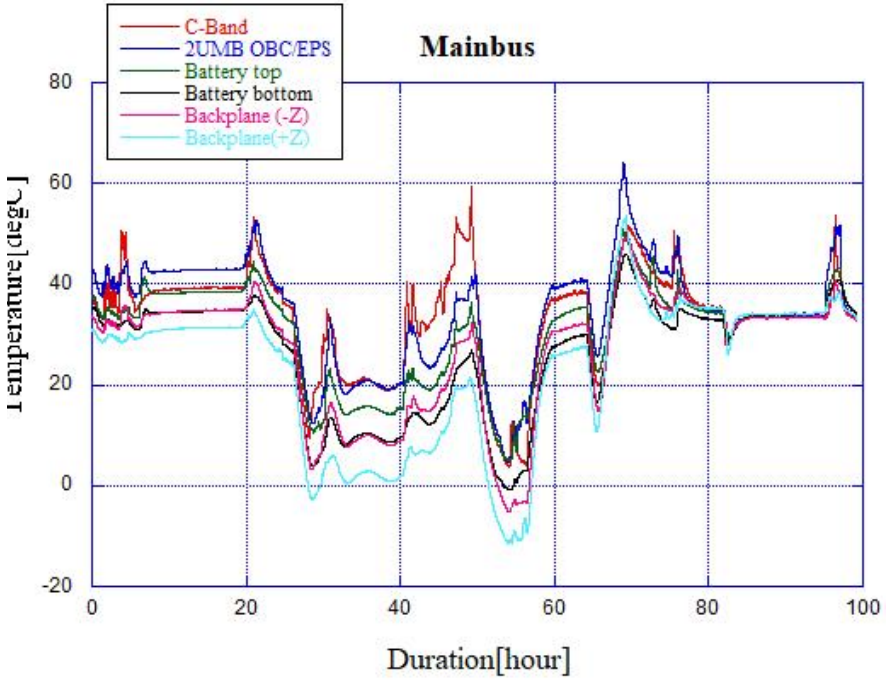


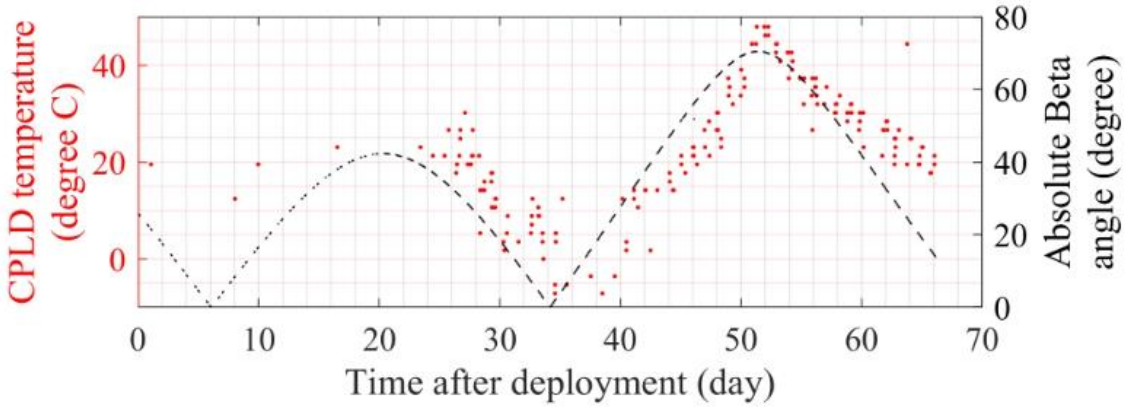
On-orbit Results: Power Consumption (2/3)



On-orbit Results: Temperature Profile (3/3)







- Similar CPLD temperature profile between on-orbit data and ground data
- Direct correlation between CPLD temperature and sun beta angle